CLAIMS

What is claimed is:

1. A method for forming a phase change memory structure comprising:

providing a substrate comprising a conductive area;

forming a spacer having a partially exposed sidewall region at an upper portion of the spacer defining a phase change memory element contact area; and,

wherein the spacer bottom portion partially overlaps the conductive area.

2. The method of claim 1, wherein the step of forming a spacer comprises the steps of:

forming a spin-on-layer (SOL) over the spacer; and,

removing a portion of the SOL to uncover an upper portion of the spacer to define an electrode contact area for a phase changing memory element.

3. The method of claim 1, wherein the spacer comprises a phase changing material sensitive to temperature.

4. The method of claim 3, wherein the phase changing material comprises a chalcogenide.

5. The method of claim 4, wherein the chalcogenide comprises a material selected from the group consisting of Ge, Te, and Sb and their alloy system.

6. The method of claim 3, further comprising the step of forming an upper conductive electrode on the electrode contact area.

7. The method of claim 6, wherein the upper conductive electrode comprises a material selected from the group consisting of W, TiN, TiW, TiAl, TiAlN, and combinations thereof.

8. The method of claim 1, wherein the spacer comprises a conductive material.

9. The method of claim 8, wherein the conductive material comprises a material selected from the group consisting of W, TiN, TiW, TiAl, TiAlN, and combinations thereof.

10. The method of claim 8, further comprising the steps of:

forming a phase changing memory element on the electrode contact area; and,

forming an upper conductive electrode on the phase changing memory element.

11. The method of claim 10, wherein the phase changing memory element comprises a chalcogenide.

12. The method of claim 11, wherein the chalcogenide comprises a material selected from the group consisting of Ge, Te, and Sb.

13. The method of claim 10, wherein the upper conductive electrode comprises a material selected from the group consisting of W, TiN, TiW, TiAl, TiAlN, and combinations thereof.

14. The method of claim 1, wherein the spacer is formed adjacent a sidewall of a dielectric insulating portion.

15. The method of claim 14, wherein the dielectric insulating portion is formed partially overlapping the conductive area.

16. The method of claim 14, wherein the dielectric insulating portion is formed spaced apart from the conductive area.

17. The method of claim 14, wherein the dielectric insulating portion comprises silicon oxide selected from the group consisting of PECVD oxide, PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, low-K dielectric, and fluorine doped silicate glass (FSG).

18. The method of claim 2, wherein the SOL layer is selected from the group consisting of organic and inorganic materials.

19. The method of claim 18, wherein the SOL layer is selected from the group consisting of spin-on-glass, benzocyclobutene (BCB), and polyimides.

20. The method of claim 2, wherein the step of removing comprises an etchback process selected from the group consisting of a wet etching and a dry etching process.

21. A method for forming a phase change memory structure comprising:

providing a substrate comprising a conductive area;

forming a spacer having a positive radius of curvature at an upper portion of the spacer and the spacer bottom portion partially overlapping the conductive area, the spacer comprising a material selected from the group consisting of a temperature sensitive phase changing material and a conductive material;

forming a spin-on-layer (SOL) over the spacer; and,

removing a portion of the SOL to uncover an upper portion of the spacer to define an electrode contact area for a phase changing memory element.

22. A phase change memory structure comprising:

a substrate comprising a conductive area;

a spacer having a partially exposed sidewall region at the spacer upper portion defining a phase change memory element contact area;

wherein the spacer bottom portion partially overlaps the conductive area;

23. The phase change memory structure of claim 22, wherein the

spacer comprises a phase changing material sensitive to temperature.

24. The phase change memory structure of claim 22, wherein the phase changing material comprises a chalcogenide.

25. The phase change memory structure of claim 24, wherein the chalcogenide comprises a material selected from the group consisting of Ge, Te, and Sb and their alloy system.

26. The phase change memory structure of claim 23, further comprising an upper conductive electrode on the electrode contact area.

27. The phase change memory structure of claim 26, wherein the upper conductive electrode comprises a material selected from the group consisting of W, TiN, TiW, TiAl, TiAlN, and combinations thereof.

28. The phase change memory structure of claim 22, wherein the spacer comprises a conductive material.

29. The phase change memory structure of claim 28, wherein the conductive material comprises a material selected from the group consisting of W, TiN, TiW, TiAl, TiAlN, and combinations thereof.

30. The phase change memory structure of claim 28, further comprising:

a phase changing memory element sensitive to temperature on the electrode contact area; and,

an upper conductive electrode on the phase changing memory element.

31. The phase change memory structure of claim 30, wherein the phase changing memory element comprises a chalcogenide.

32. The phase change memory structure of claim 31, wherein the chalcogenide comprises a material selected from the group consisting of Ge, Te, and Sb and their alloy system.

33. The phase change memory structure of claim 30, wherein the upper conductive electrode comprises a material selected from the group consisting of W, TiN, TiW, TiAl, TiAlN, and

combinations thereof.

34. The phase change memory structure of claim 22, wherein the spacer is disposed adjacent a sidewall of a dielectric insulating portion.

35. The phase change memory structure of claim 34, wherein the dielectric insulating portion is disposed partially overlapping the conductive area.

36. The phase change memory structure of claim 34, wherein the dielectric insulating portion is disposed spaced apart from the conductive area.

37. The phase change memory structure of claim 34, wherein the dielectric insulating portion comprises silicon oxide selected from the group consisting of PECVD oxide, PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, low-K dielectric, and fluorine doped silicate glass (FSG).

38. The phase change memory structure of claim 22, wherein the SOL layer is selected from the group consisting of organic and inorganic materials.

39. The phase change memory structure of claim 22, wherein the SOL layer is selected from the group consisting of spin-on-glass, benzocyclobutene (BCB), and polyimides.

40. A phase change memory structure comprising:

a substrate comprising a conductive area; and,

a spacer having a partially exposed positive radius of curvature at the spacer upper portion defining a phase change memory element contact area, the spacer comprising a material selected from the group consisting of a conductive material and a phase change material sensitive to temperature;

wherein the spacer bottom portion partially overlaps the conductive area.